REMARKS/ARGUMENTS

In the above-identified Office Action, the Examiner rejected all pending claims under 35 U.S.C. §103(a). These rejections are discussed below.

Claims 17 and 31 have been amended to further clarify the subject matter regarded as the invention. Claims 9-16, 26-30, and 33-38 are now cancelled without prejudice. Claims 1-8, 17-25, 31-32, and 39 remain pending in this application.

Reconsideration of the application is respectfully requested based on the amendments and the following remarks.

REJECTION OF ALL PENDING CLAIMS 1UNDER 35 U.S.C. §103

In the Office Action, the Examiner rejected claims 1-8 under 35 U.S.C. §103(a) as being unpatentable over Bartley (U.S. Patent No. 6,219,796, hereinafter "*Bartley*") in view of Fletcher et al. (U.S. Patent No. 6,611,920, hereinafter "*Fletcher*"); rejected claims 9-16 over Bartley in view of *Fletcher* and *Matter et al.* (U.S. Patent No. 5,392,437, hereinafter "*Matter*"); rejected claim 17-25 over *Matter* in view of *Bartley*, *Fletcher* and *Sproch et al.* (U.S. Patent No. 6,247,134, hereinafter "*Sproch*"); rejected claims 26 and 28-36 over *Bartley* in view of *Fletcher* and *Sproch*; rejected claim 37 over *Matter* in view of *Bartley*, *Fletcher* and *Sproch*; and rejected claim 39 over *Bartley*, *Fletcher*, and *Simonvich* (U.S. Patent 6,308,241, hereinafter "*Simonvich*"). These rejections are discussed below.

The present invention pertains to methods and systems for saving power in pipelined processors. **Claims 1-8 and 39** have been rejected under 35 U.S.C. §103(a) as being unpatentable over *Bartley* in view of Fletcher and will be addressed first.

Discussion of Claims 1-8 and 39

The Action offers (for example, at item 5, on page 1) that *Bartley* teaches a "microprocessor including a functional unit [11] formed of a plurality of stages [functional units]. This statement is perhaps at the heart of the differences between the claimed invention and the cited art. As is known to those having ordinary skill in the art, when a functional unit processes an instruction it executes the instruction using a sequential process of a series of "stages" that when completed comprise the

full execution of the instruction by the functional unit. All of the cited references discuss the operation and control of power to entire functional units. None of the references discuss selective control of power to the specific stages that make up the functional units.

Adding to the confusion is the misuse of the term "functional unit" by *Bartley*. This is explained as follows. Item 11 of *Bartley* is rather a CPU core containing functional unit blocks, or more importantly, datapaths (11d or 11e) that each contain several functional units (e.g., L1, S1, M1, D1, See, also Bartley at 5:35-40) that perform specific operations on selected instruction types. These are the functional units described in the present invention and the cited art. Thus, the functional units (e.g., L1, S1, M1, D1) are not sequentially operating stages of a functional unit, but rather are parallel functional units such as depicted in the present invention (See, e.g., 106 of Fig. 1 or 302 of Fig. 3 and so on).

Moreover, *Bartley* does not depict or otherwise describe the stage operation of any of the functional units. The cited portions of *Bartley* (3:1-30 and 3:41-65) describe a process for shutting down of entire functional units (See, e.g., Bartley at 5:50-60). *Bartley* selectively turns these functional units on and off to save power when the functional units are not needed. This is a rough method of power control. The specification of the instant application describes this pre-existing methodology in some degree of detail. Accordingly, *Bartley* has absolutely no applicability to the present invention and is not properly employed in an obviousness type rejection. The cited art discloses no understanding of the fact that even though a functional unit can be "on", power can still be saved by selectively turning off the power to selected stages of the "on" functional unit. This is a radical departure from the prior art. The same lack of granular power control is also present in *Fletcher* (see, for example, 3:47-52). The present specification goes into great detail describing precisely the limitations of methodologies like that of *Bartley* and *Fletcher*.

An advantage of the present invention is explained as follows. During the operation of a functional unit the instruction passes through a sequence of stages used to execute the instruction using the functional unit (Figs. 5, 6A-6E illustrate this). The instruction is processed sequentially through each of these stages using a clocked sequence of steps that advance the processing in accord with the clock pulses of the microprocessor. Thus, the functional unit executes a series of steps (stages) during the time the functional unit uses to process a given instruction. The inventors have noted that when an instruction is processed by a functional unit, for most of the stages, no operations

are required. They have also determined that the various stages of a functional unit can be turned off without turning off all power to the entire functional unit. Thus, other stages still in use are powered while the power is off to the stages not processing (for example, those processing no-op's instruction steps). This allows power to be selectively supplied to only the needed stages and the non-operational stages go without power. This allows finer granularity of power control and saves even more power than the ideas suggested by *Bartley* and *Fletcher*.

Thus, both the cited portions of *Fletcher* and *Bartley* describe systems for turning off entire functional units instead of turning the stages on and off.

Specifically, claim 1 of the present invention requires the "stages of said functional unit are arranged in series" and controlling of the supply of current to each of a plurality of stages of a functional unit after evaluating instructions and producing activity indicators, which facilitate the control of the supply of current. The method of claim 1 allows for efficient evaluation of operation type of each instruction so that power supplied to each stage of a functional unit can be individually controlled. This is done "by providing a clock signal and the activity indicators to a logic gate that determines that only selected stages of said plurality of stages will draw current from a power supply". The cited art fails to teach or suggest these limitations.

Accordingly, it is submitted that *Fletcher* and *Bartley* alone or in any combination, do not teach or suggest all the features of claim 1. In addition, it is submitted that dependent claims 2-8 & 39, are also patentably distinct from cited art for at least the same reasons as those recited above for independent claim 1. The additional limitations recited in the dependent claims are not further discussed, as the above-discussed limitations are believed to be sufficient to distinguish the claimed invention from the cited references. Thus, it is respectfully requested that the Examiner withdraw the rejection of claims 1-8 and 39.

Discussion of Claims 17-25

Claims 17-25 pertain to a microprocessor and system where an instruction evaluation unit is connected to an instruction register where the instruction evaluation unit evaluates the next instruction to produce activity indicators. Moreover, the system is claimed such that a specific implementation of a time delay is instituted between two related clock signals as explained below.

Claim 17 is amended to further claim the following limitations. For example claim 17 recites **a memory unit having an "amount of time required to registering an output comprises time T_r", "a stage activation controller clock pulse C_{SR}"** and a time for advancing markers **"through a shift register of the stage activation controller such that it takes time T_s to advance each marker a shift register in the stage activation controller", and "a clock circuit that supplies a stage activation controller clock pulse C_{SR} to said stage activation controller and also provides a functional unit clock pulse C_{FU} to said functional unit wherein the clock pulse C_{FU} is subject to a gate delay of time T_g, and wherein said functional unit clock pulse C_{FU} is time-delayed with respect to said stage activation controller clock pulse C_{SR} by an amount of time greater than the sum of times T_s, T_r, and T_g thereby enabling the respective stage of the functional unit to have its power status adjusted depending the requirements of the instruction entering said respective stage"**.

This precise degree of time control is not taught or suggested in *Fletcher*. Moreover, *Matter* does not remedy this deficiency nor does the other applied reference *Sproch*. Accordingly, the applicants believe that above-discussed limitations are sufficient to distinguish the claimed invention from the cited references. Therefore, the applicants further submit that the cited art fails to establish a prima facie case of obviousness. Accordingly, it is respectfully requested that the Examiner withdraw the rejection of Claim 17. And for at least the same reasons applicants respectfully request that the rejections of dependent Claims 18-25 also be withdrawn.

Claims 31 & 32

The amendment of Claim 31 is merely an incorporation of the base limitations of Claim 26 into Claim 31 which is now independent. As to Claim 31 and dependent Claim 32 the applicants argue that the cited ground of rejection does not teach all elements of the claims. For example, the applicants believe that the rejection made does not teach or suggest "**a stage activation controller that utilizes said activity indicators and causes each of said stages of said functional unit to be**

individually activated or deactivated stage wherein said stage activation controller is a memory unit that stores said activity indicators". It is argued that *Fletcher* (at 4:17-19) teaches a memory unit operating as a stage activation controller. Examination of the cited portions of *Fletcher* reveal that the cited portions of *Fletcher* teach only teach NAND gates and a "propagation circuit" without any reference or suggestion of a memory circuit. Accordingly, the proffered ground of rejection is insufficient to establish a satisfactory obviousness rejection. Moreover, as this claim merely incorporates the limitations of the rejected base claim (Claim 26) it is not a substantial amendment affecting patentability. Accordingly, the applicants believe that above-discussed limitations are sufficient to distinguish the claimed invention from the cited references. Therefore, the applicants further submit that the cited art fails to establish a prima facie case of obviousness. Accordingly, it is respectfully requested that the Examiner withdraw the rejection of Claim 31. And for at least the same reasons applicants respectfully request that the rejection of dependent Claim 32 also be withdrawn.

Additionally, Claims 9-16, 26-30, 33, 38 are cancelled making any discussion of these asserted grounds of rejection moot.

Based on the foregoing, it is submitted that claims 1-8, 17-25, 31-32 and 39 are patentably distinct from *Bartley, Fletcher, Matter, Sproch* and/or *Simonvich*. Thus, it is respectfully requested that the Examiner withdraw the rejection of the pending claims under 35 U.S.C § 103(a).

Conclusion

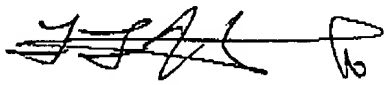
It is submitted that claims 1-8, 17-25, 31-32, and 39 are patentable distinct from the cited portions of the art relied on by the Examiner. Therefore, reconsideration of the application and an early Notice of Allowance are earnestly solicited.

If there are any issues remaining which the Examiner believes could be resolved through either a Supplemental Response or an Examiner's Amendment, the Examiner is respectfully requested to contact the undersigned attorney at the telephone number listed below.

If any fees are due in connection with the filing of this Amendment, the Commissioner is authorized to deduct such fees from the undersigned's Deposit Account No. 50-0388 (Order No. APL1P203).

Respectfully submitted,

BEYER WEAVER & THOMAS, LLP



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